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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Hao, *et al.*

Filed: 07/31/2003

Serial No.: 10/631,251

For: Method for Fabricating Poly Patterns



Attorney Docket: TSM03-0521

Examiner: TBD

Art Unit: TBD

Commissioner for Patents  
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*Kristin Hayes*  
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*8/19/03*  
Date

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Respectfully submitted,

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**INFORMATION DISCLOSURE  
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Sheet 1 of 1

**Complete if Known**

Application Number	10/631,251
Filing Date	July 31, 2003
First Named Inventor	Hao, et al.
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	TSM03-0521

**U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number Number - Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
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**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>

**OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	A	Wu, C.C., et al., "A 90-nm CMOS Device Technology with High-Speed, General-Purpose, and Low-Leakage Transistors for System on Chip Applications," IEDM (February 2002) pp. 65-68.	

Examiner Signature	Date Considered
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